

FIG. 2 is a schematic diagram of a system 200, including a first node 1 and a second node N, each having a processor 240 and a memory 242. The first node 1 is connected to a first input 1 and a first output 1. The second node N is connected to a second input M and a second output M. The first node 1 and the second node N are connected to each other via a network 248. The first node 1 and the second node N are also connected to a common bus 244. The first node 1 and the second node N are also connected to a common bus 246.

200

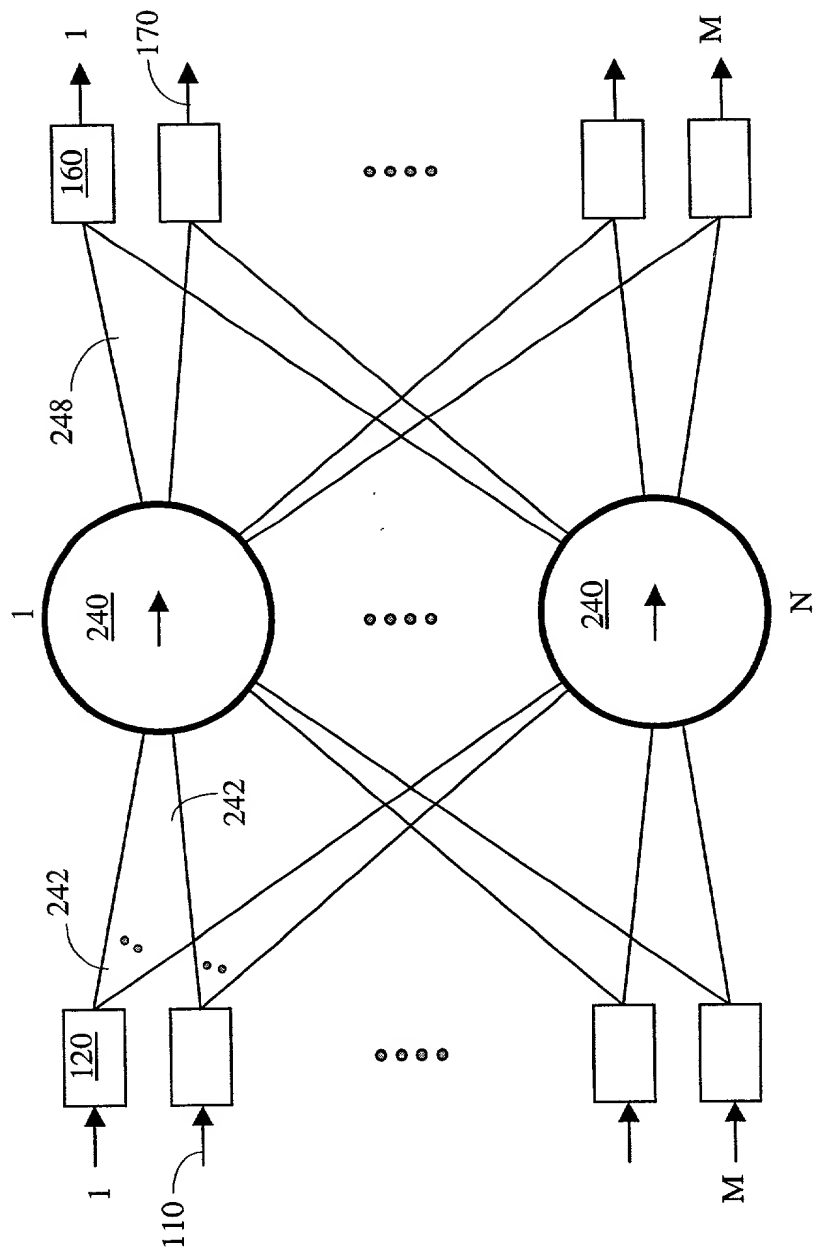


Fig. 2

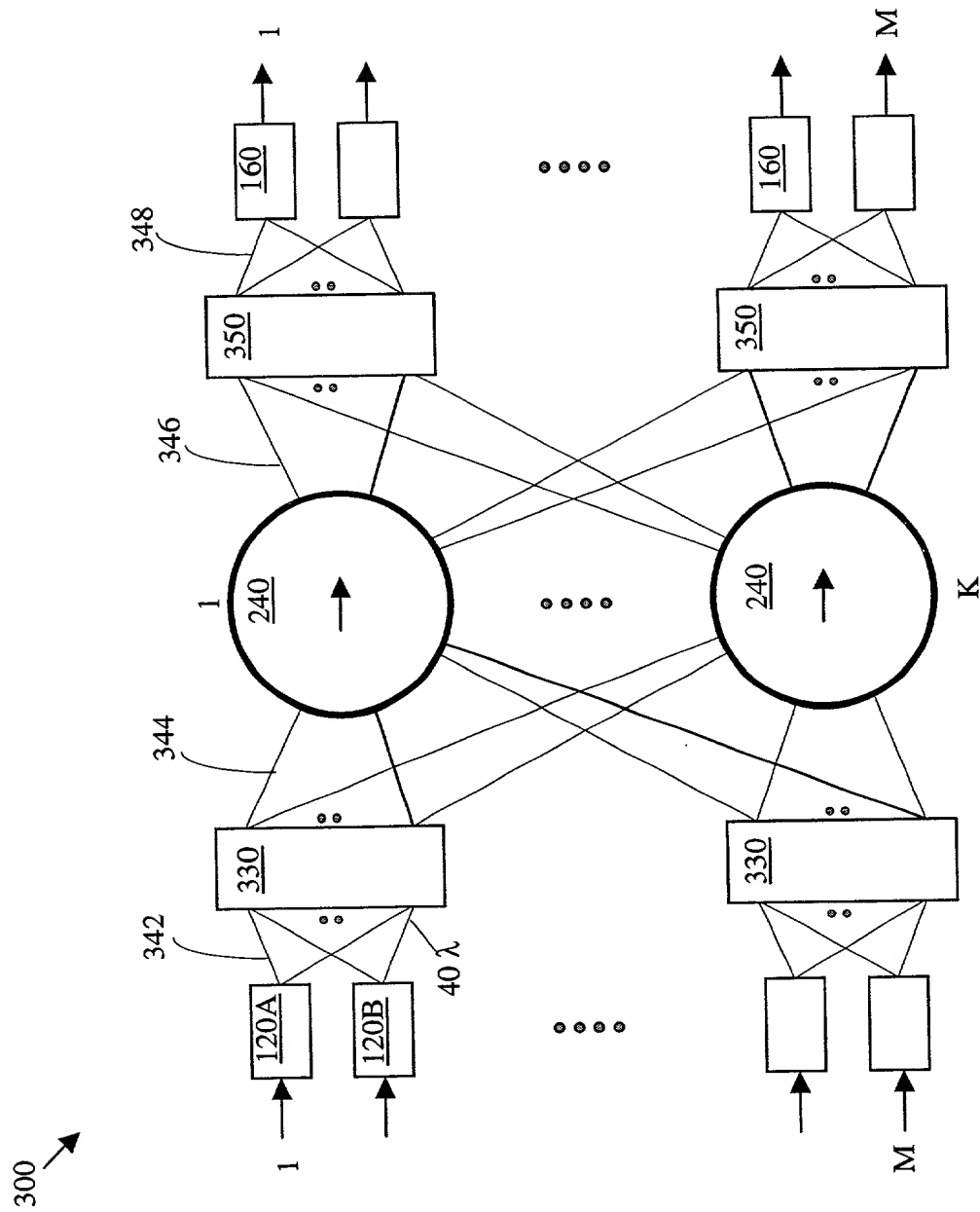


Fig. 3

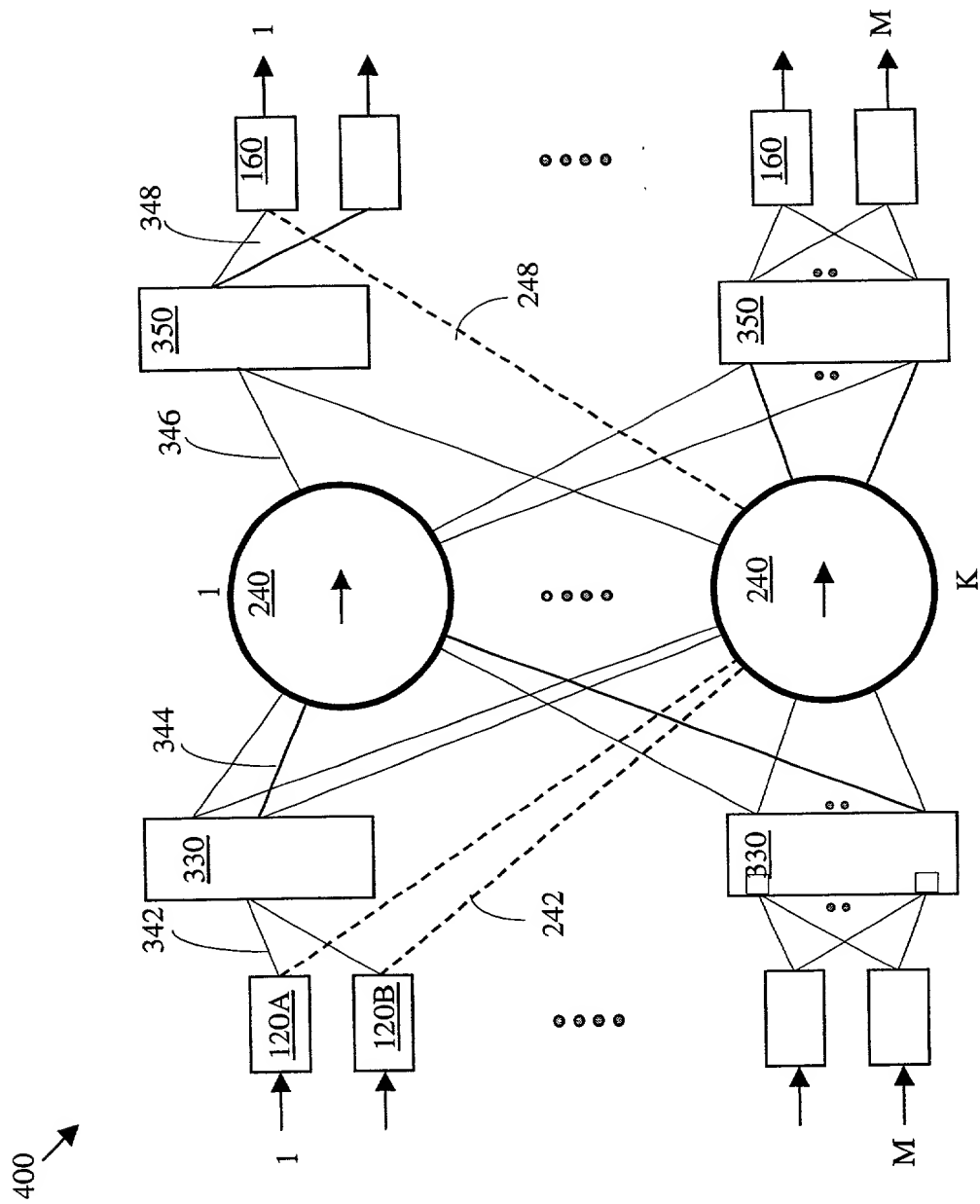


Fig. 4

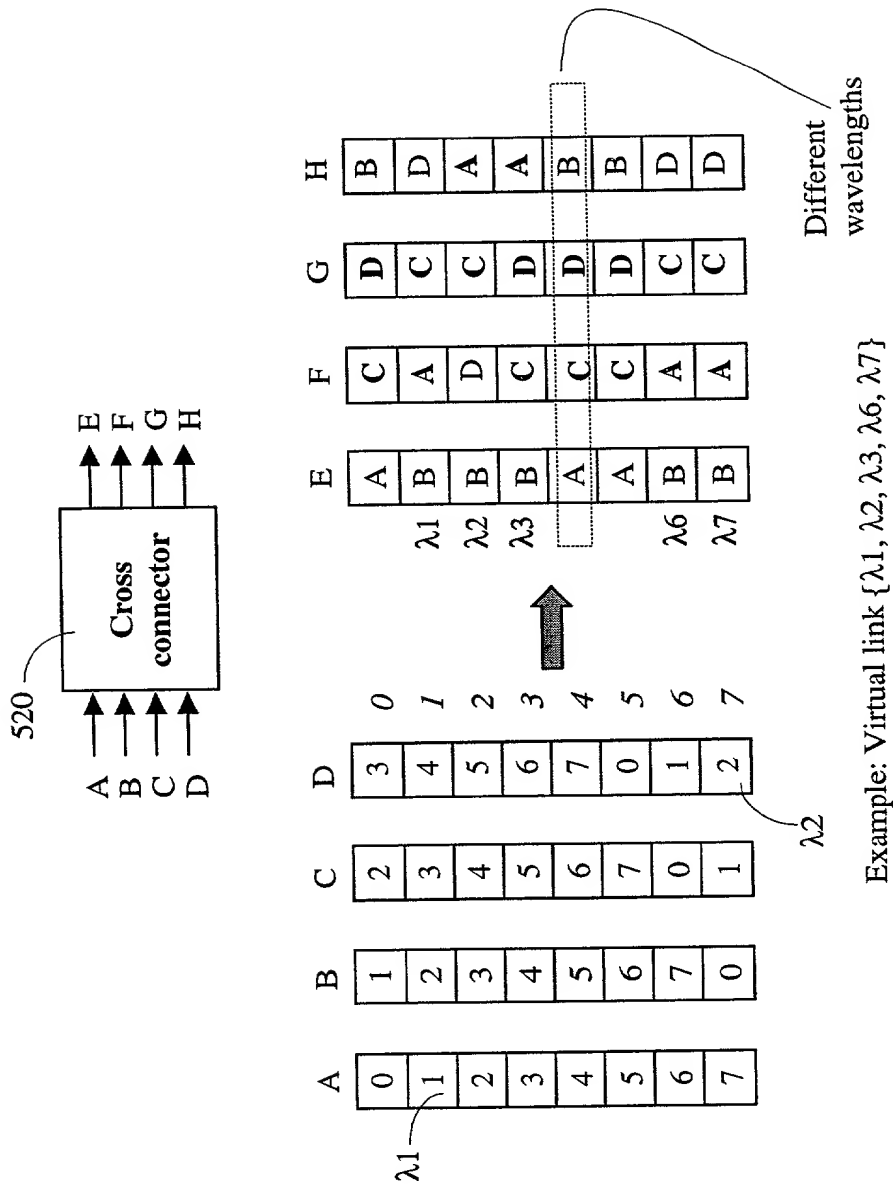


Fig. 5

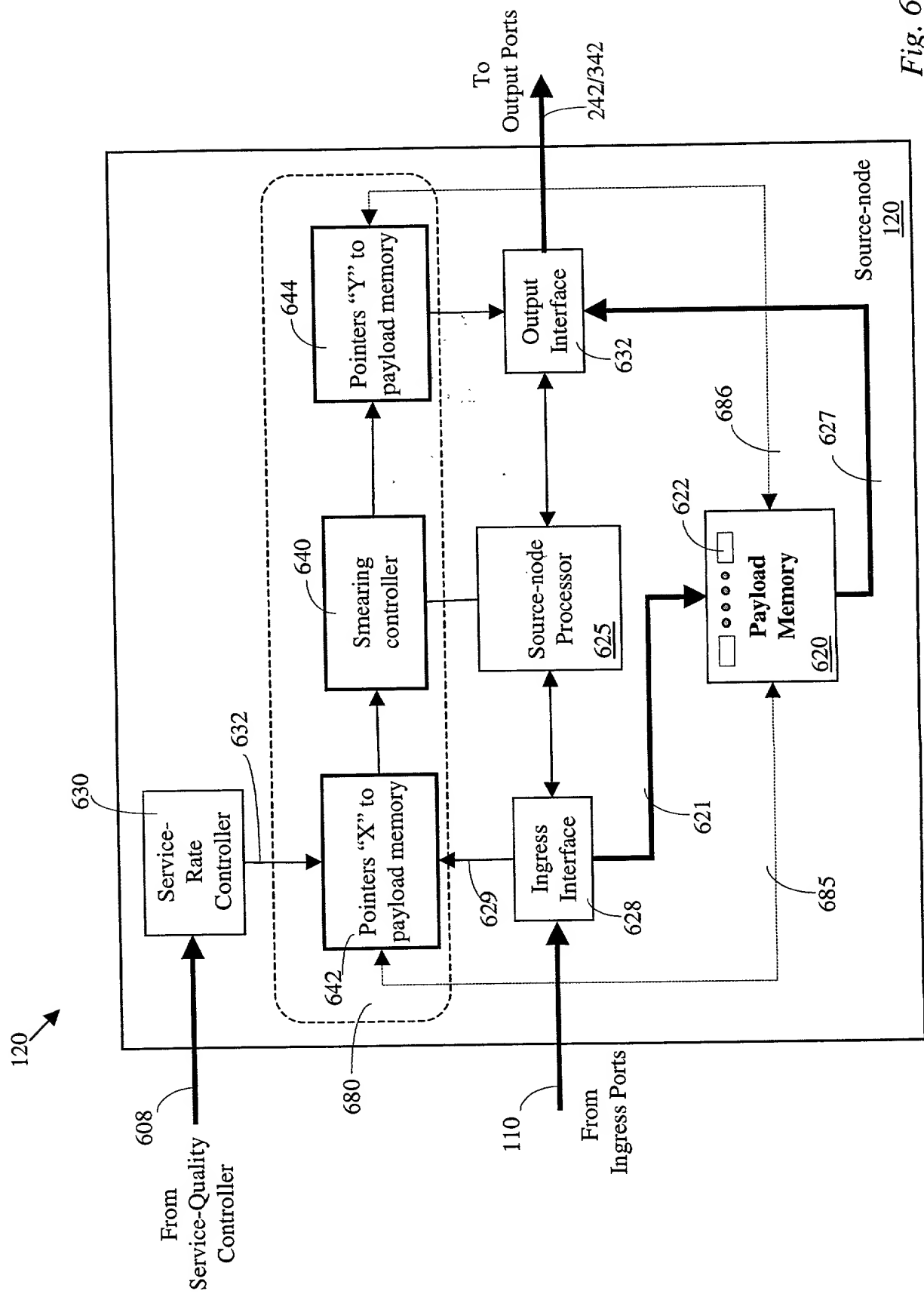


Fig. 6

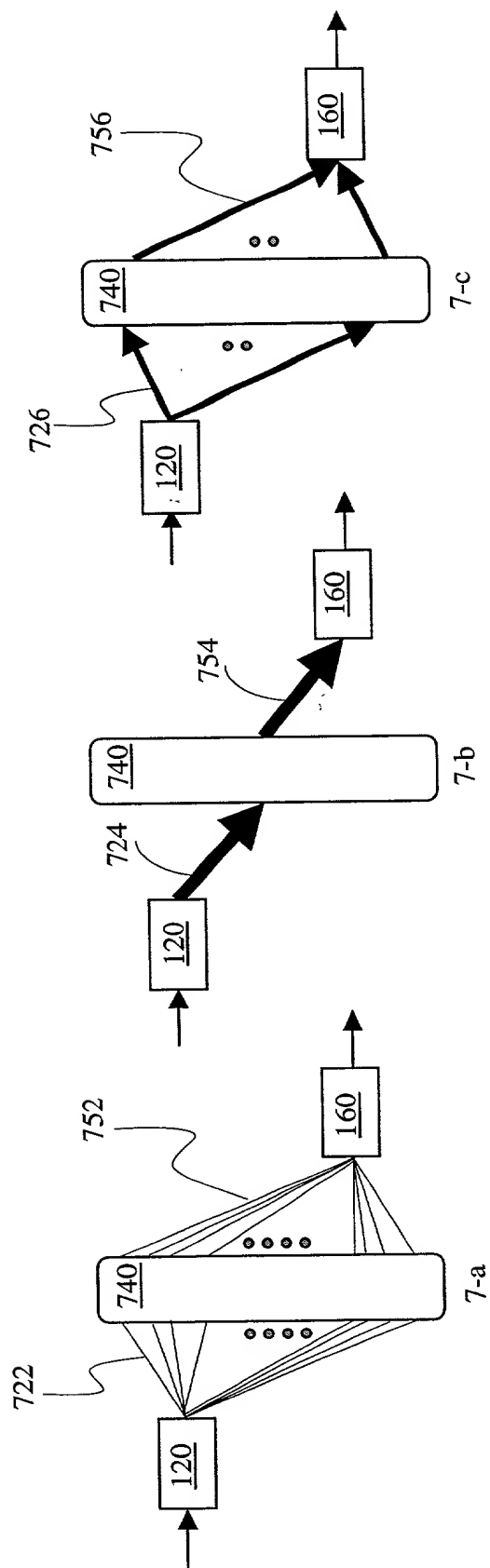


Fig. 7

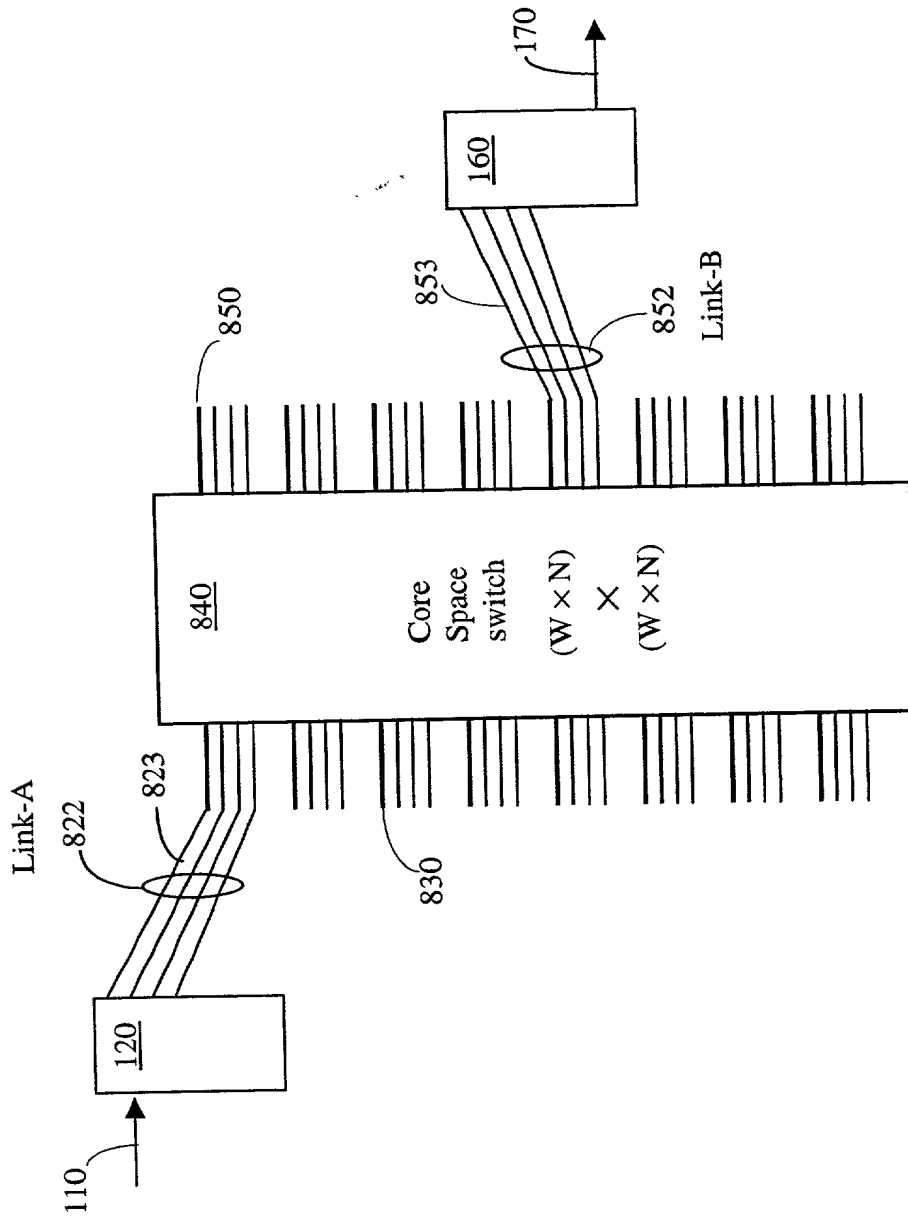


Fig. 8

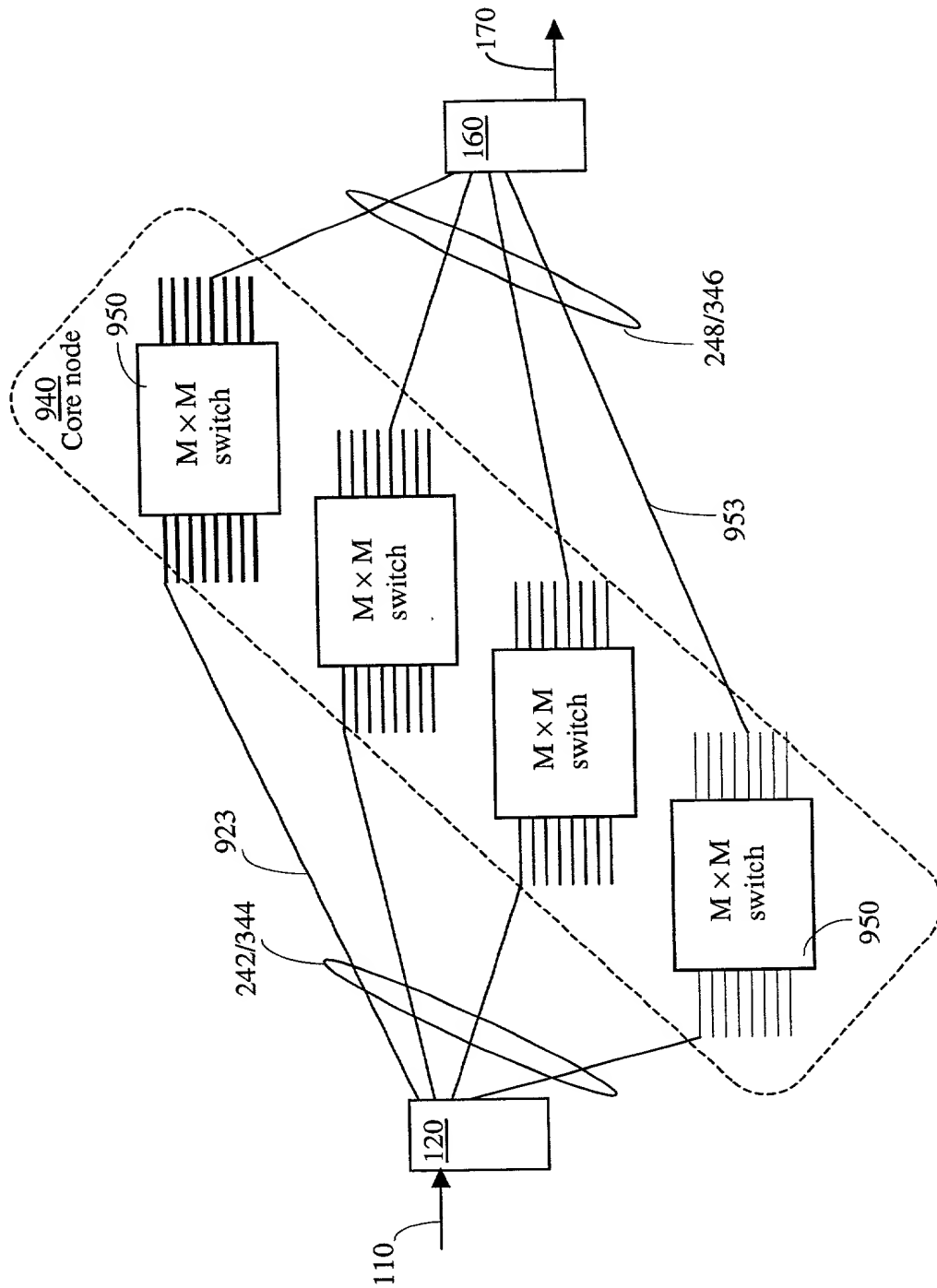


Fig. 9

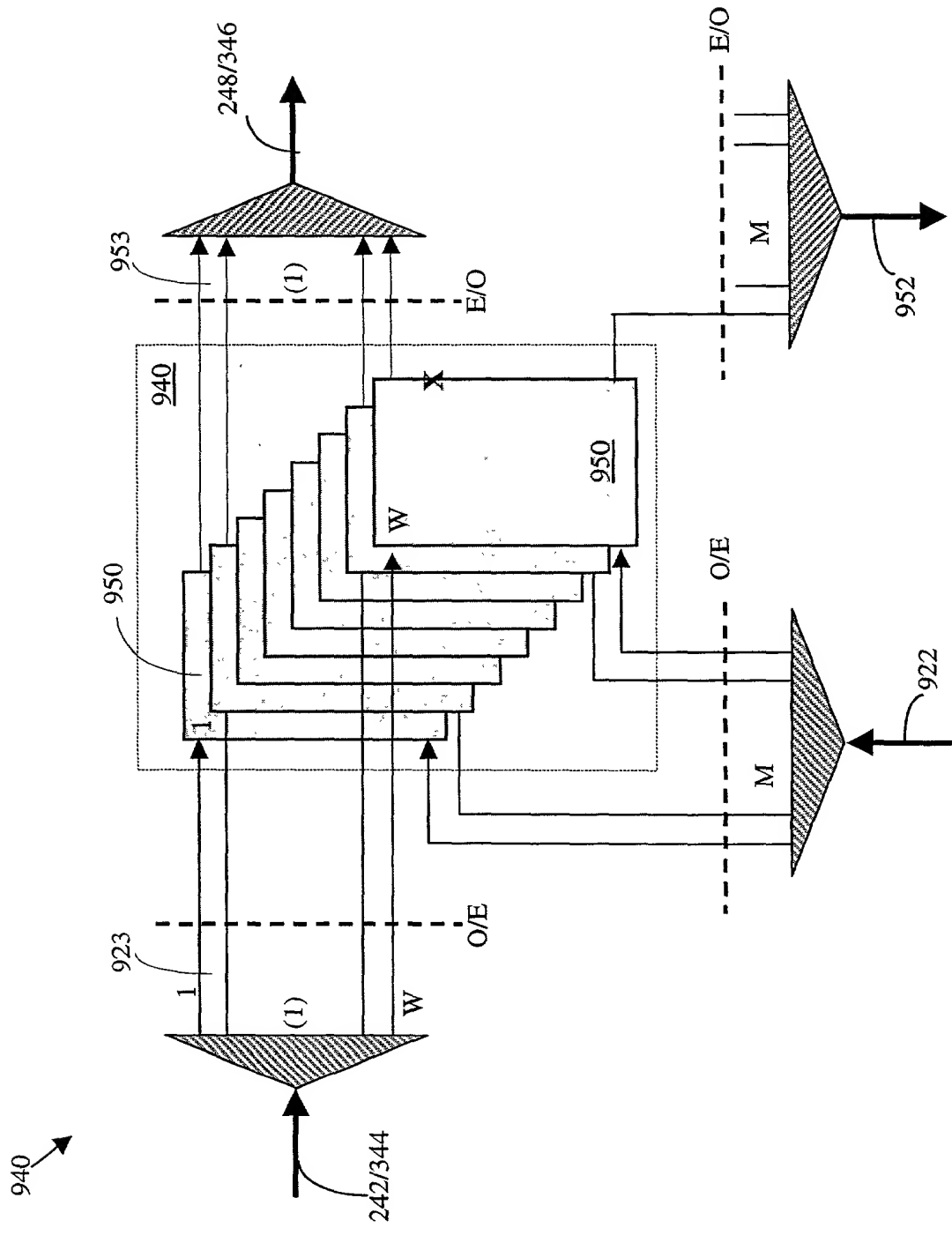


Fig. 10

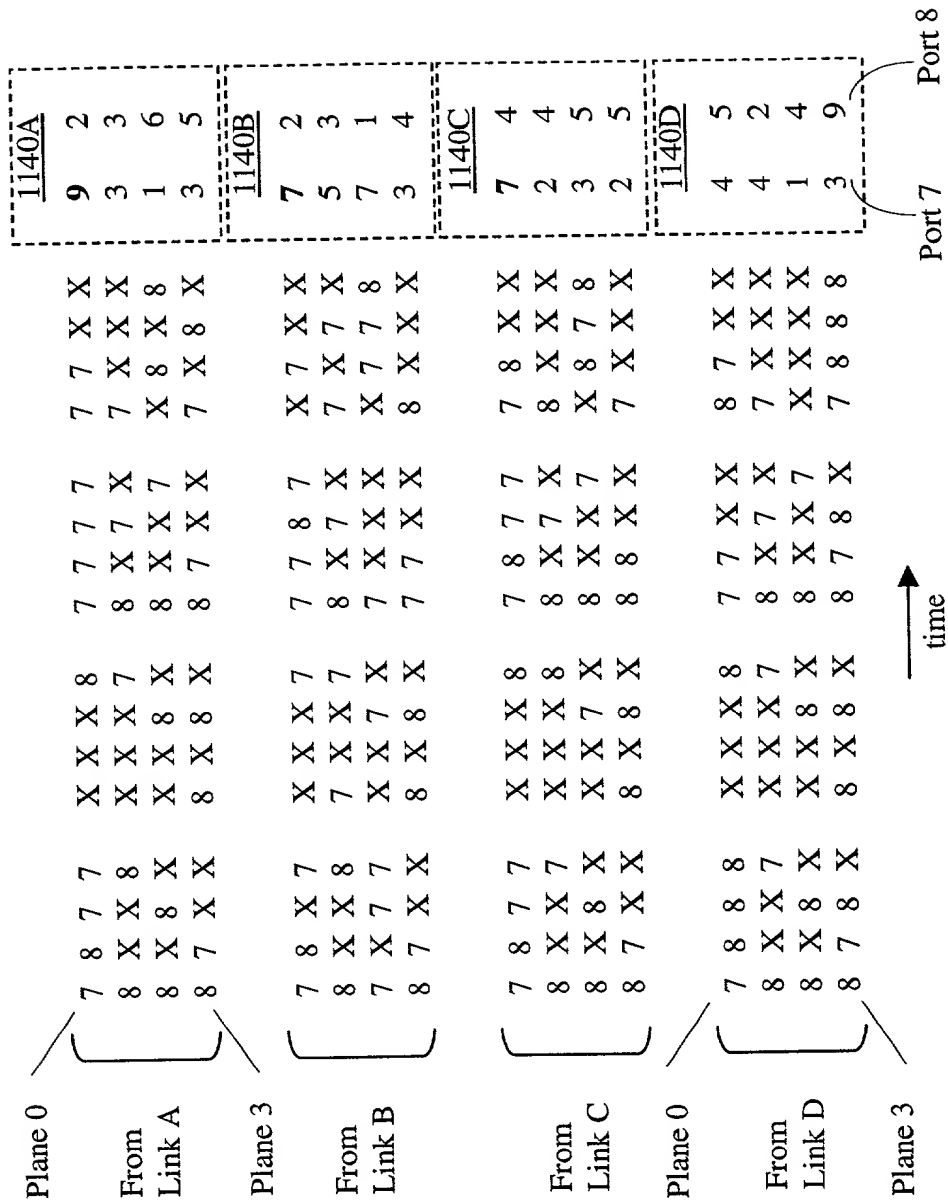


Fig. 11a

1160 ↗

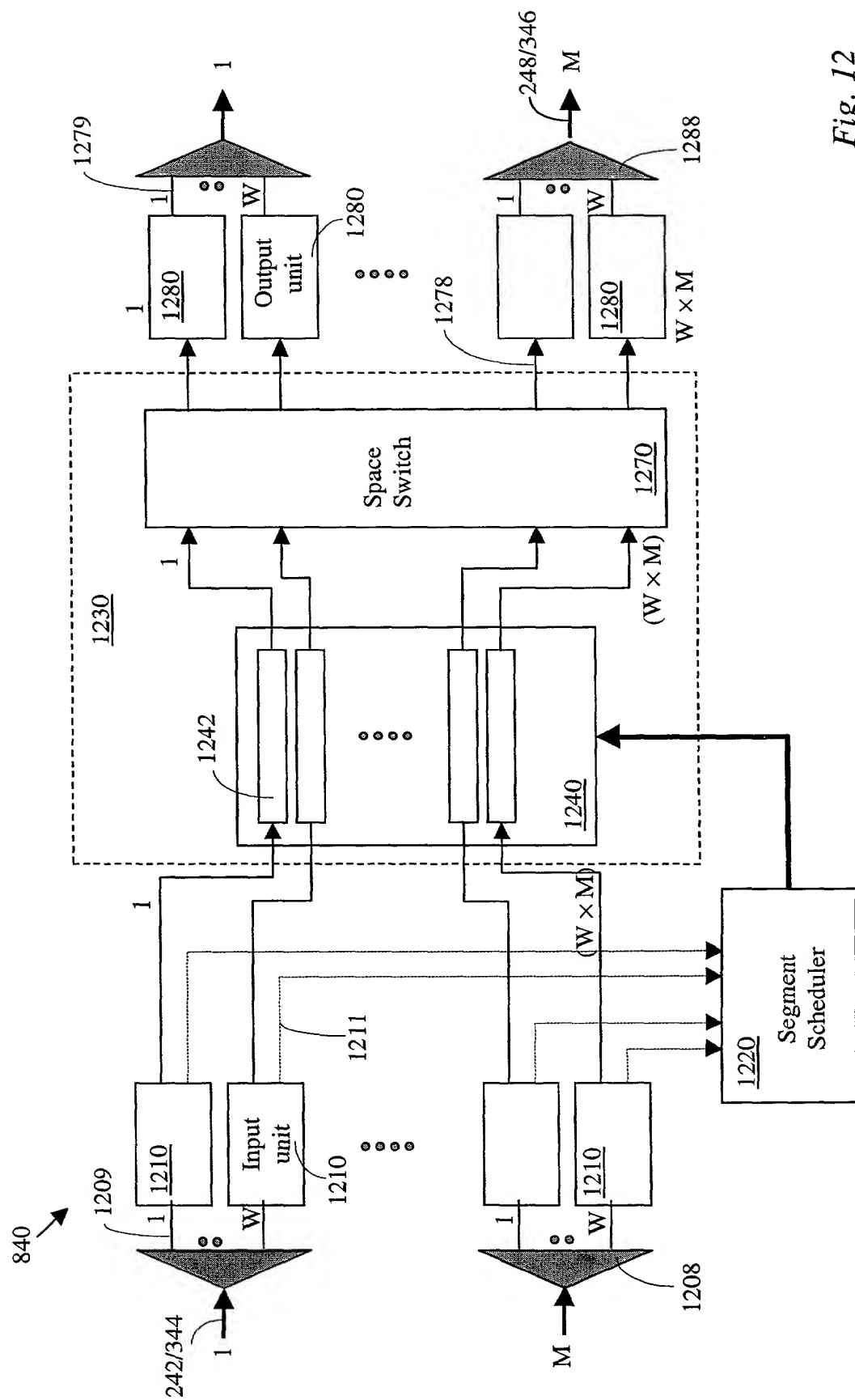
	Port 7	Port 8
Link-A	16	16
Link-B	22	10
Link-C	14	18
Link-D	12	20
	64	64

Fig. 11b

1180 ↘

	Port 7	Port 8
Plane-0	27	13
Plane-1	14	12
Plane-2	12	16
Plane-3	11	23
	64	64

Fig. 11c



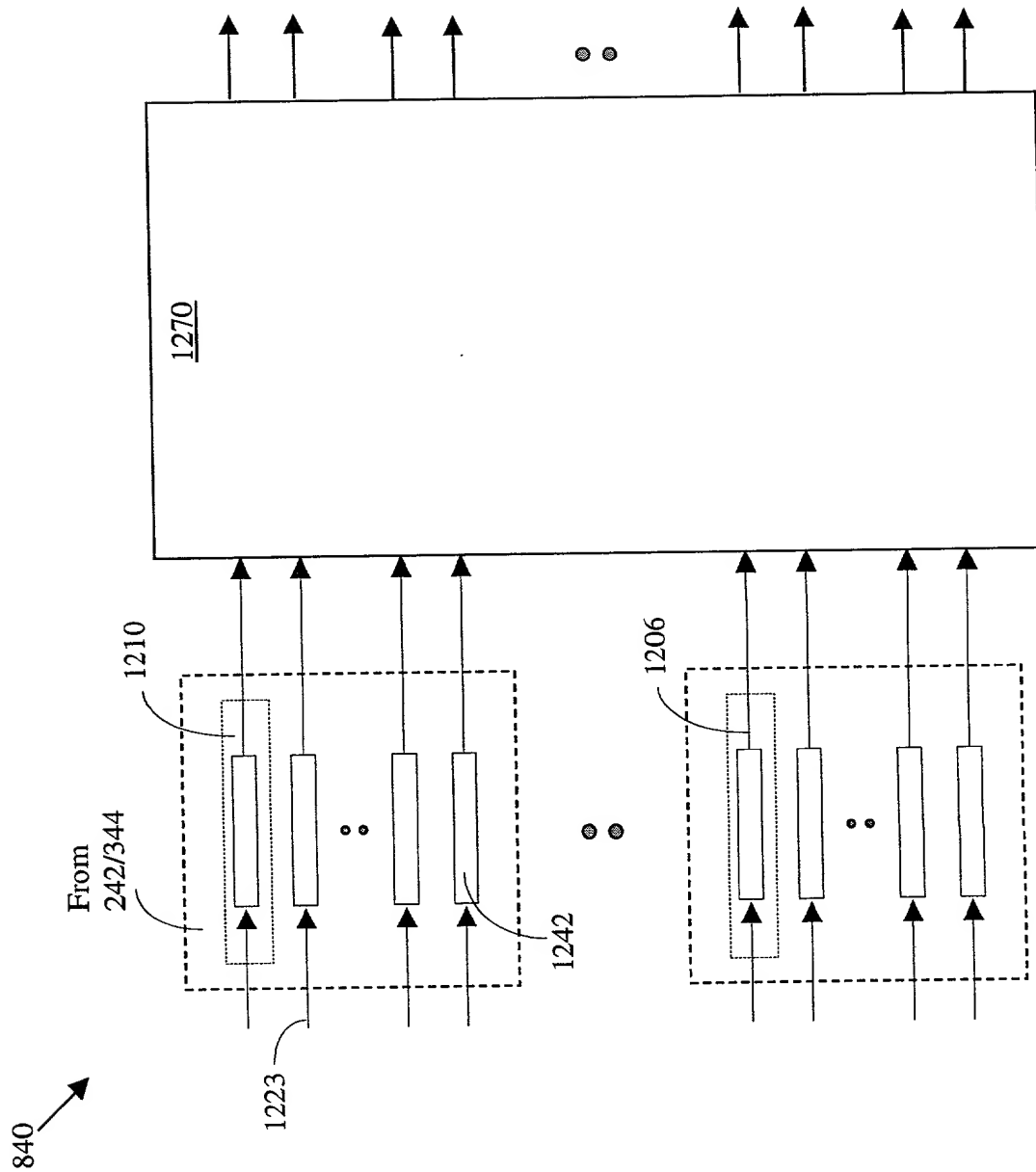


Fig. 13

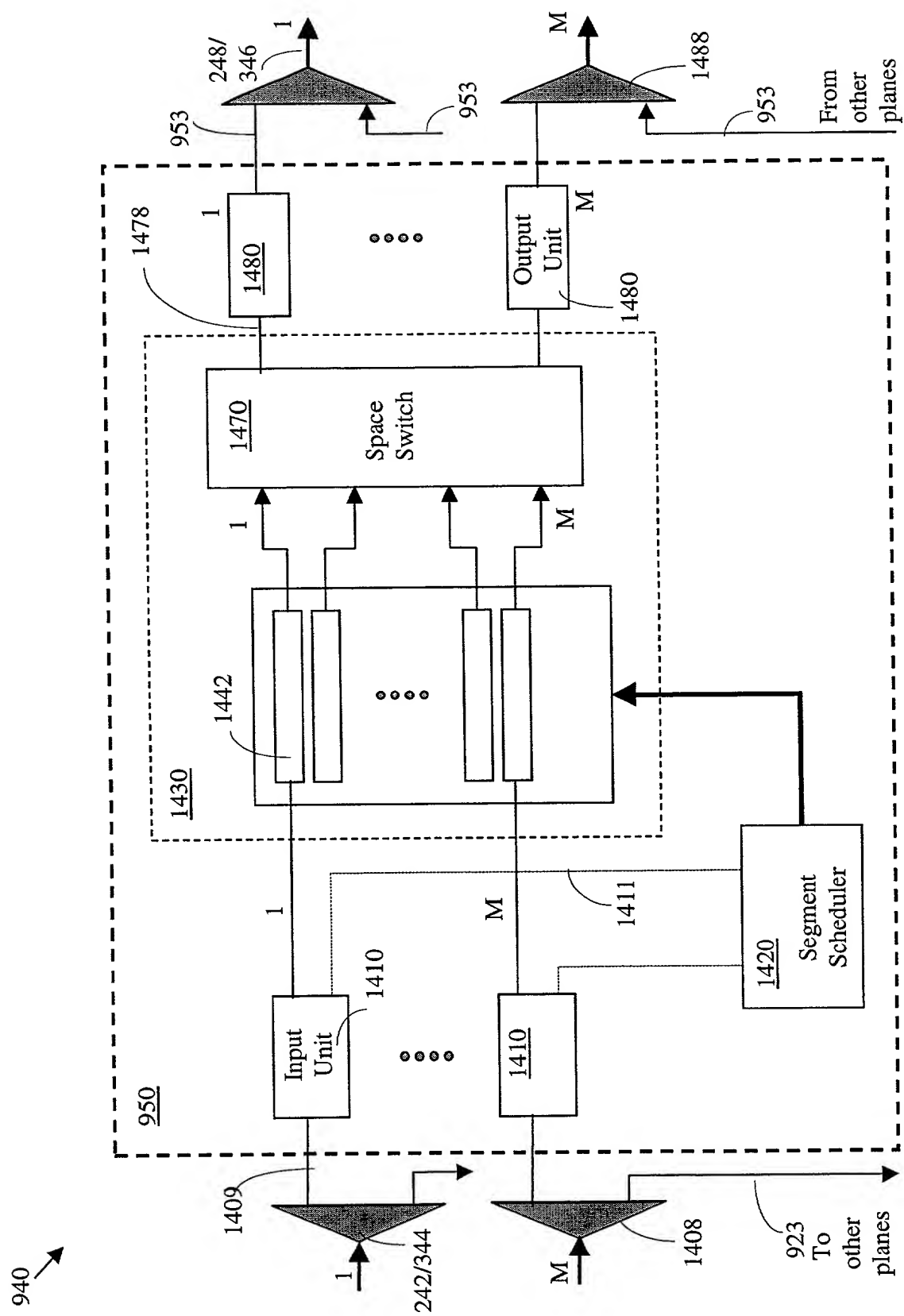


Fig. 14

FIG. 15 is a block diagram of a system 1430, including a first processing unit 1442 and a second processing unit 1478, each receiving input from a corresponding input device 1470. The first processing unit 1442 is connected to the second processing unit 1478 via a communication link 1470. The system 1430 is configured to process data received from the input devices 1470 and output the results to the output devices 1478.

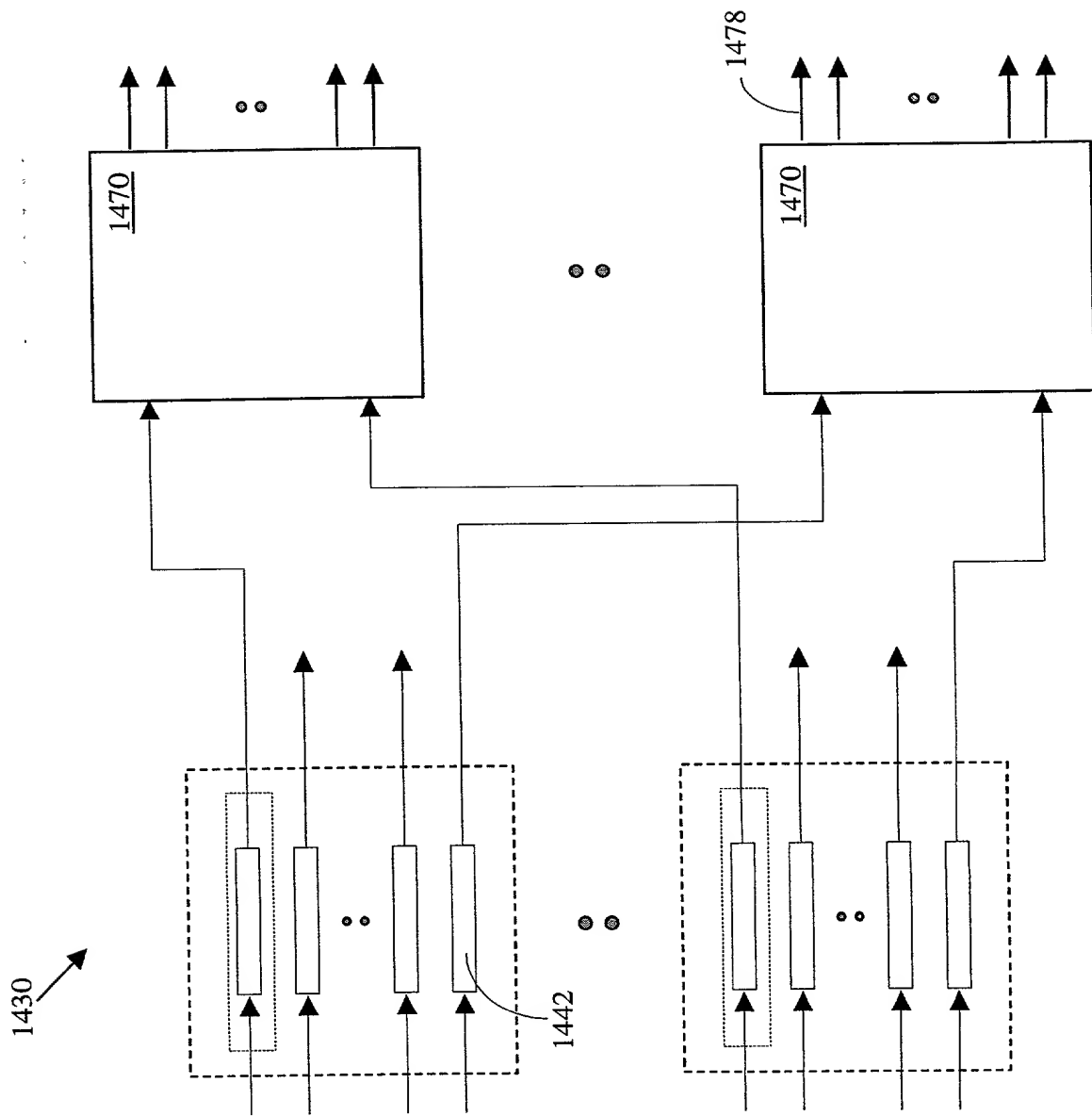


Fig. 15

FIG. 16 is a schematic diagram of a network topology. The network consists of a source node (1600) and a sink node (1602). The source node is connected to a first link (1604) and a second link (1606). The first link (1604) is connected to a first node (1608) and a second node (1610). The second link (1606) is connected to a third node (1612) and a fourth node (1614). The first node (1608) is connected to the second node (1610) and the third node (1612). The second node (1610) is connected to the third node (1612) and the fourth node (1614). The third node (1612) is connected to the fourth node (1614) and the sink node (1602). The sink node (1602) is connected to the fourth node (1614).

1600

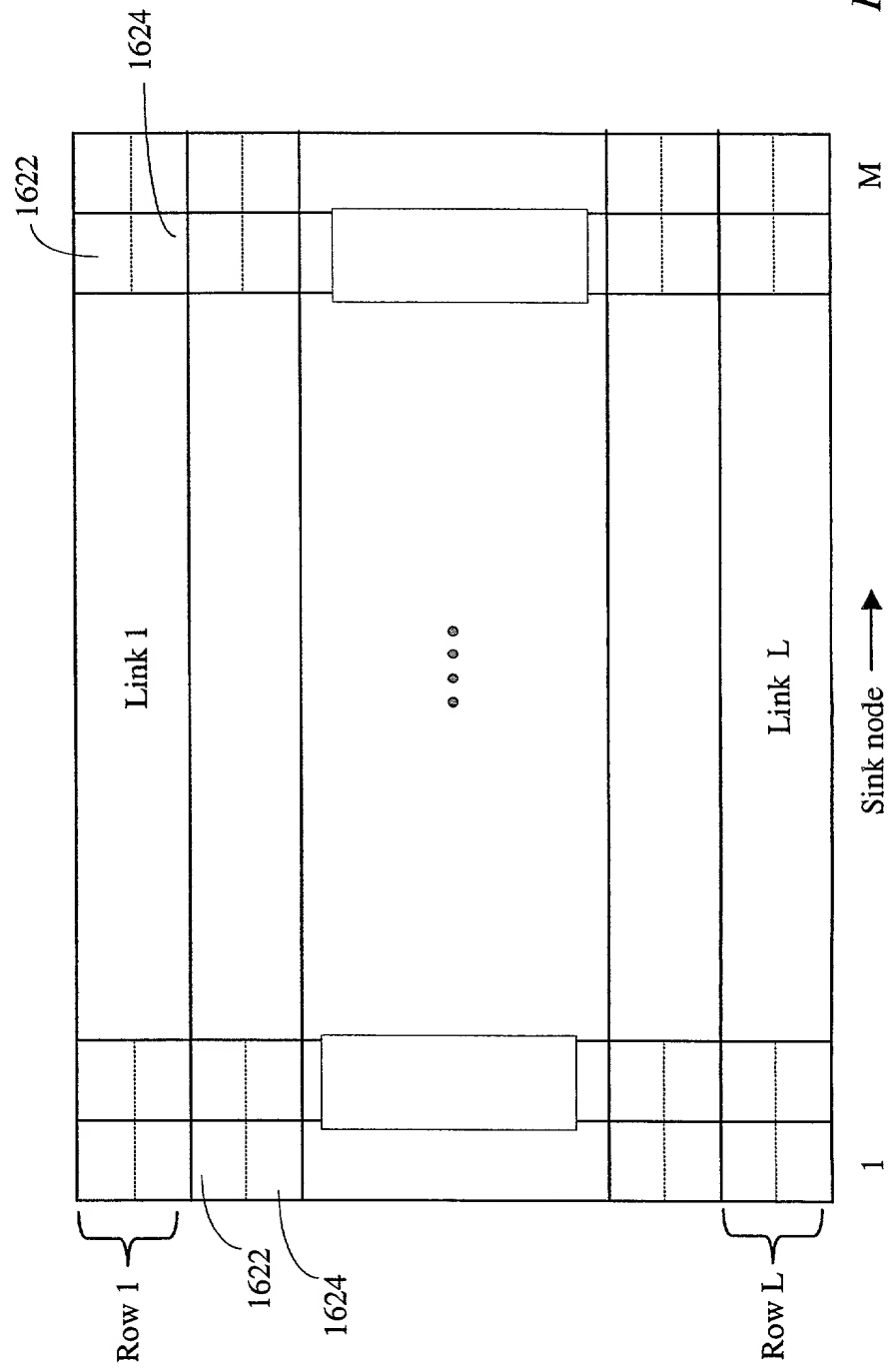


Fig. 16

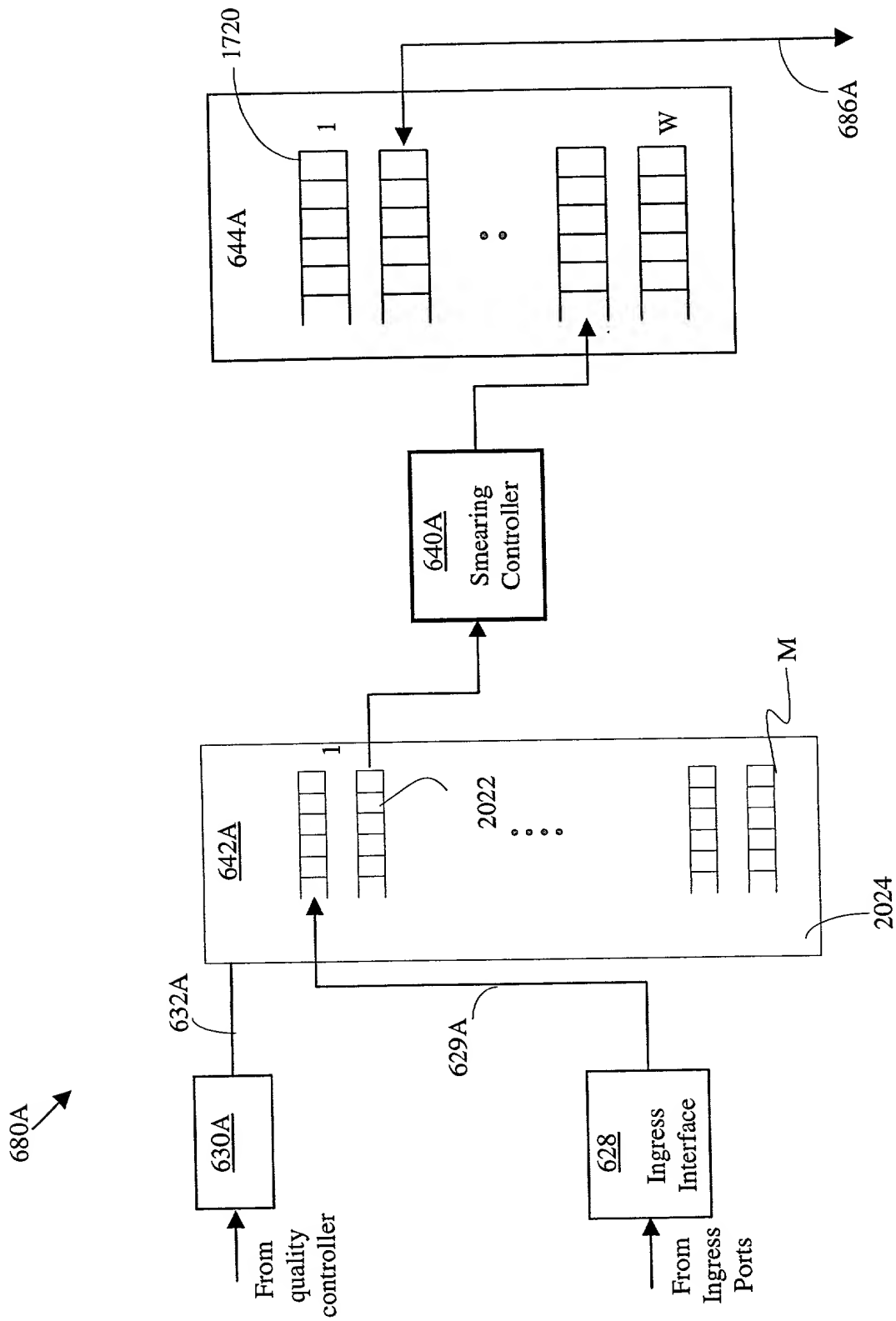


Fig. 17



FIG. 18 is a block diagram of a system 1800 for selecting a channel for a link. The system 1800 includes a processor 1810, a memory 1820, and a communication interface 1830. The processor 1810 is configured to receive a request for a link from a user device 1840. The processor 1810 is also configured to determine a set of available channels for the link. The processor 1810 is further configured to select a channel from the set of available channels based on a selection criterion. The processor 1810 is then configured to provide the selected channel to the user device 1840 via the communication interface 1830.

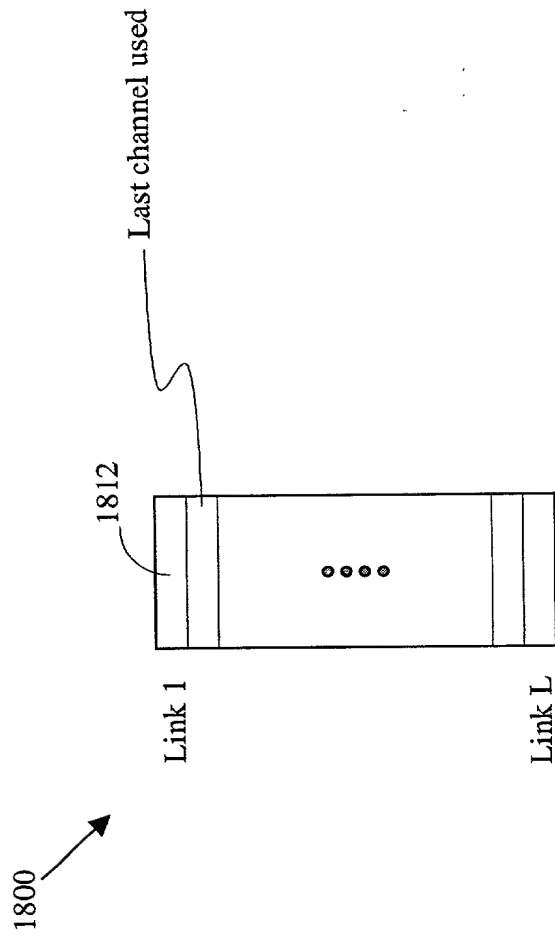


Fig. 18



FIG. 19 is a schematic diagram of a system 1900, which includes a plurality of links 1920, each having a plurality of segments 1922. The links 1920 are connected to a central hub 1924, which is configured to receive and transmit data to the links 1920. The links 1920 are arranged in a circular pattern around the central hub 1924.

1900

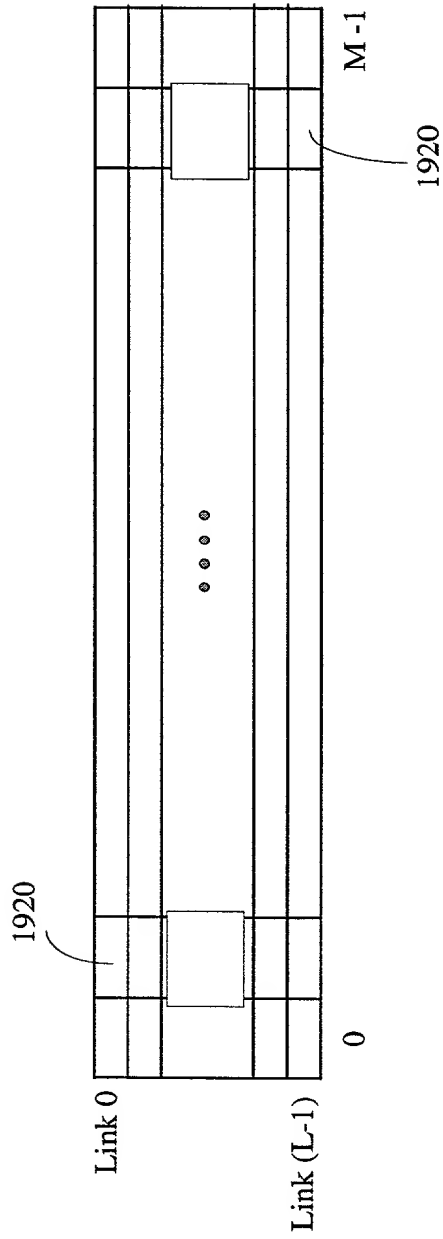


Fig. 19